

**AMENDMENTS TO THE CLAIMS**

**This listing of claims will replace all prior versions and listings of claims in the application:**

**LISTING OF CLAIMS:**


1. (Original) A base station or a mobile station of a radio-operated telecommunications system with a receiver for processing received information and with at least one digital processor, in particular a digital signal processor, for performing a symbol rate processing, the signal processor being suitable for and provided for likewise performing at least parts of a chip rate processing.

2. (Original) A base station or a mobile station as claimed in Claim 1, the signal processor being suitable for performing a task allocation for controlling the chip rate processing and the symbol rate processing.

3. (Original) A base station or a mobile station as claimed in Claim 1, the signal processor being designed such that firstly the chip rate processing and then the symbol rate processing can be performed.

4. (Original) A base station or mobile station as claimed in Claim 1, wherein an array or group of digital signal processors is provided.

5. (Original) A base station or a mobile station as claimed in Claim 4, wherein the chip rate processing and the symbol rate processing can be distributed between sub-arrays or sub-groups of signal processors.



6. (Original) A base station or a mobile station as claimed in Claim 1, wherein at least one memory is provided which is suitable for and provided for the intermediate storage of the received information.

7. (Original) A base station or a mobile station as claimed in Claim 1, wherein the chip rate processing is comprising a despreading of the received information.

8. (Original) A base station or a mobile station as claimed in Claim 1, the symbol rate processing comprising a decoding of the received information.

9. (Original) A receiver for a base station or a mobile station of a radio-operated telecommunications system for processing received information with at least one digital processor, in particular a digital signal processor, for performing a symbol rate processing, wherein the signal processor is suitable for and provided for likewise performing at least parts of a chip rate processing.

10. (Previously Presented) A radio-operated telecommunications system, wherein a base station or a mobile station as claimed in Claim 1 is provided.

11. (Original) A telecommunications system as claimed in Claim 10, consisting of a code division multiple access (CDMA) telecommunications system.

12. (Original) A process for operating a radio-operated telecommunications system, wherein information received by a base station or a mobile station is subjected to a symbol rate processing by means of at least one digital processor, in particular a digital signal processor, wherein at least a part of the chip rate processing is likewise performed by the at least one signal processor.

13. (Original) A process as claimed in Claim 12, wherein firstly the chip rate processing and then the symbol rate processing is performed.

14. (Original) A process as claimed in Claim 12, wherein a task allocation for controlling the chip rate processing and the symbol rate processing is performed by the at least one signal processor.

15. (Original) A process as claimed in Claim 12, wherein an array or group of digital signal processors is provided, the chip rate processing and the symbol rate processing is distributed between sub-arrays or sub-groups of signal processors.

16. (Original) A process as claimed in Claim 15, wherein the distribution of the array or group of signal processors between the chip rate processing and the symbol rate processing is performed by the task allocation.

17. (Previously Presented) A radio-operated telecommunications system, wherein a receiver as claimed in Claim 9 is provided.

18. (New) Digital processor, in particular digital signal processor, for performing a symbol rate processing for a receiver of a base station or a mobile station of a radio-operated telecommunications system, wherein the signal processor is suitable for and provided for performing additionally at least parts of a chip rate processing.

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